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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,248	01/14/2004	Jimmie Earl DeWitt JR.	AUS920030544US1	: 6475

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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,248	DEWITT ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER 4/4/2006
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04 & 7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 1/14/2004 and 7/1/2005 was considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Element 260 of figure 2. It is also of note that due to the number of figures not all of the elements of the figures have been checked to see if they are mentioned in the description and the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

The cross-reference to related applications section of the specification is incomplete.

Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1, 3, 7, 13, 15, 19, and 25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. There are no tangible end results from implementing the claims in question because the end result is a determination or an identification, which both lack a tangible "real world" result.

Although some claims do have intermediate steps that produce an intermediate tangible result, the end result still lacks tangibility.

Claims 13-24 are also directed to non-statutory subject matter because of an improper definition of acceptable computer readable media. Such forms of unacceptable computer readable media include the disclosed "radio frequency and light wave transmissions" detailed on page 27 in the submitted specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Burrows (U.S. Patent # 5,887,159), herein referred to as Burrows.

As per claim 1, Burrows discloses a method in a data processing system for processing instructions, the method comprising:

responsive to receiving an instruction at a processor in the data processing system (See column 2, lines 49-59: Instructions are fetched, decoded and executed), determining whether an indicator is associated with the instruction (See column 2, lines 59-65: This is done by checking to see if hint information is null or not);

enabling counting, by the processor, of each event associated with execution of the instruction if the indicator is associated with the instruction (See figure 5 and column 5, lines 11-13: A count field is available for keeping track of the number of times a certain action occurs), wherein the processor autonomically increments the count of the events associated with execution of the instruction in a hardware counter (A counter inherently is able to increment a count when certain operations occurs);

determining if the count of the events associated with the execution of the instruction stored in the hardware counter meets or exceeds a threshold (See column 5, lines 14-17: Counts are tracked and used to update hint information); and

identifying a portion of code associated with the instruction as being a hot spot if the count of the events associated with the execution of the instruction in the hardware counter meets or exceeds the threshold (See column 5, lines 29-30: The best_hint field indicates the current hot spot).

As per claim 2, Burrows discloses wherein the instruction is received in an instruction cache in the processor (See column 4, lines 3-5: An instruction cache is present).

As per claim 3, Burrows discloses wherein the indicator is stored in a performance instrumentation shadow cache (See figure 5: A hint prediction table is used to store information) and wherein the processor checks the performance instrumentation shadow cache to determine whether the indicator is associated with the

instructions (See column 2, lines 59-65: This is done by checking to see if hint information is null or not).

As per claim 4, Burrows discloses wherein the instruction is received in a bundle by an instruction cache in the processor (See column 4, lines 3-5: An instruction cache block implies instructions are received in a bundle) and wherein the indicator comprises at least one spare bit in a field in the bundle (See figure 2: The figure shows an instruction with a hint field).

As per claim 5, Burrows discloses wherein the indicator is a separate instruction (See figures 2 and 5, and column 4 lines 18-25: The presence of a hint field changes how instructions are interpreted and thus can be treated as a separate instruction).

As per claim 6, Burrows discloses wherein an event in the events includes at least one of an entry into a module (See column 2, lines 53-54: All code is placed into object code modules), an exit from a module (The code must exit the module to be executed), an entry into a subroutine (See column 3, lines 38-40: Subroutines are used), an exit from a subroutine (Code must inherently exit subroutines at some point—either by natural degradation or interrupt), an entry into a function (See column 3, lines 41-42: Procedures are functions), an exit from a function (Code must inherently exit functions at some point—either by natural degradation or interrupt), a start of input/output (See column 3, lines 14-22: Data is read/passed along), a completion of

input/output (This must stop before an instruction can be executed properly), and the execution of the instruction (All meaningful instructions inherently executed).

As per claim 7, Burrows discloses wherein the determining step comprises:

determining, by an instruction cache, whether the indicator is present in a field within the instruction (See column 2, lines 59-65: This is done by checking to see if hint information is null or not).

As per claim 8, Burrows discloses wherein the enabling step comprises:

sending a signal to a performance monitor unit (See column 2, lines 62: A signal is sent to generate a monitor program), wherein the performance monitor unit counts each event associated with execution of the instruction using the hardware counter (See figure 5 and column 5, lines 11-13: Counters are used when a monitor program dictates so).

As per claim 9, Burrows discloses wherein identifying a portion of code associated with the instruction as being a hot spot includes:

generating, in the processor, an interrupt (See column 5, lines 11-13: Intercepting an execution involves interrupting it); and

sending the interrupt to an interrupt handler of a performance monitoring application (See column 5, lines 11-13: This has to be inherently done with a interception else nothing would happen).

As per claim 10, Burrows discloses wherein the performance monitoring application, upon receiving the interrupt, performs an action associated with the identification of a hot spot in the instructions (See column 5, lines 31-52: The hint can be changed when appropriate).

As per claim 11, Burrows discloses wherein the action includes:

storing the portion of code corresponding to the hot spot in a shadow data structure (See column 5, lines 1-8: A hint prediction table stores instructions and hint information); and

generating a mapping from old addresses associated with the portion of code to new addresses of the portion of code in the shadow data structure (See column 4, lines 64-67: Mapping is done with the aid of hint fields in the hint prediction table).

As per claim 12, Burrows discloses wherein the action includes at least one of generating a performance monitoring application log entry and notifying a log daemon process (See column 5, lines 53-58: A log entry is made saving any register use before an interception which is done by the monitor procedures, which are log daemon processes).

As per claim 13, Burrows discloses a computer program product (See column 2, lines 47-49: The instructions come from code) in a computer readable medium for processing instructions comprising:

first instructions for determining whether an indicator is associated with an instruction in response to receiving the instruction at a processor in the data processing system (See column 2, lines 59-65: This is done by checking to see if hint information is null or not);

second instructions for enabling counting, by the processor, of each event associated with execution of the instruction if the indicator is associated with the instruction (See figure 5 and column 5, lines 11-13: A count field is available for keeping track of the number of times a certain action occurs), wherein the processor autonomically increments the count of the events associated with execution of the instruction in a hardware counter (A counter inherently is able to increment a count when certain operations occurs);

third instructions for determining if the count of the events associated with the execution of the instruction stored in the hardware counter exceeds a threshold (See column 5, lines 14-17: Counts are tracked and used to update hint information); and

fourth instructions for identifying a portion of code associated with the instruction as being a hot spot if the count of the events associated with the execution of the instruction in the hardware counter exceeds the threshold (See column 5, lines 29-30: The best_hint field indicates the current hot spot).

As per claim 14, Burrows discloses wherein the instruction is received in an instruction cache in the processor (See column 4, lines 3-5: An instruction cache is present).

As per claim 15, Burrows discloses wherein the indicator is stored in a performance instrumentation shadow cache (See figure 5: A hint prediction table is used to store information) and wherein the performance instrumentation shadow cache is checked to determine whether the indicator is associated with the instructions (See column 2, lines 59-65: This is done by checking to see if hint information is null or not).

As per claim 16, Burrows discloses wherein the instruction is received in a bundle by an instruction cache in the processor (See column 4, lines 3-5: An instruction cache block implies instructions are received in a bundle) and wherein the indicator comprises at least one spare bit in a field in the bundle (See figure 2: The figure shows an instruction with a hint field).

As per claim 17, Burrows discloses wherein the indicator is a separate instruction (See figures 2 and 5, and column 4 lines 18-25: The presence of a hint field changes how instructions are interpreted and thus can be treated as a separate instruction).

As per claim 18, Burrows discloses wherein an event in the events includes at least one of an entry into a module (See column 2, lines 53-54: All code is placed into

object code modules), an exit from a module (The code must exit the module to be executed), an entry into a subroutine (See column 3, lines 38-40: Subroutines are used), an exit from a subroutine (Code must inherently exit subroutines at some point—either by natural degradation or interrupt), an entry into a function (See column 3, lines 41-42: Procedures are functions), an exit from a function (Code must inherently exit functions at some point—either by natural degradation or interrupt), a start of input/output (See column 3, lines 14-22: Data is read/passed along), a completion of input/output (This must stop before an instruction can be executed properly), and the execution of the instruction (All meaningful instructions inherently executed).

As per claim 19, Burrows discloses wherein the first instructions include instructions for determining, by an instruction cache, whether the indicator is present in a field within the instruction (See column 2, lines 59-65: This is done by checking to see if hint information is null or not).

As per claim 20, Burrows discloses wherein the second instructions for enabling include instructions for sending a signal to a performance monitor unit (See column 2, lines 62: A signal is sent to generate a monitor program), wherein the performance monitor unit counts each event associated with execution of the instruction using the hardware counter (See figure 5 and column 5, lines 11-13: Counters are used when a monitor program dictates so).

As per claim 21, Burrows discloses wherein the fourth instructions for identifying a portion of code associated with the instruction as being a hot spot include:

instructions for generating, in the processor, an interrupt (See column 5, lines 11-13: Intercepting an execution involves interrupting it); and

instructions for sending the interrupt to an interrupt handler of a performance monitoring application (See column 5, lines 11-13: This has to be inherently done with a interception else nothing would happen).

As per claim 22, Burrows discloses wherein the performance monitoring application, upon receiving the interrupt, performs an action associated with the identification of a hot spot in the instructions (See column 5, lines 31-52: The hint can be changed when appropriate).

As per claim 23, Burrows discloses wherein the action includes:

storing the portion of code corresponding to the hot spot in a shadow data structure (See column 5, lines 1-8: A hint prediction table stores instructions and hint information); and

generating a mapping from old addresses associated with the portion of code to new addresses of the portion of code in the shadow data structure (See column 4, lines 64-67: Mapping is done with the aid of hint fields in the hint prediction table).

As per claim 24, Burrows discloses wherein the action includes at least one of generating a performance monitoring application log entry and notifying a log daemon process (See column 5, lines 53-58: A log entry is made saving any register use before an interception which is done by the monitor procedures, which are log daemon processes).

As per claim 25, Burrows discloses an apparatus for processing instructions comprising:

means for determining whether an indicator is associated with an instruction in response to receiving the instruction (See column 2, lines 59-65: This is done by checking to see if hint information is null or not) at a processor in the data processing system (See column 2, lines 49-59: Instructions are fetched, decoded and executed);

means for enabling counting, by the processor, of each event associated with execution of the instruction if the indicator is associated with the instruction (See figure 5 and column 5, lines 11-13: A count field is available for keeping track of the number of times a certain action occurs), wherein the processor autonomically increments the count of the events associated with execution of the instruction in a hardware counter (A counter inherently is able to increment a count when certain operations occurs);

means for determining if the count of the events associated with the execution of the instruction stored in the hardware counter exceeds a threshold (See column 5, lines 14-17: Counts are tracked and used to update hint information); and

means for identifying a portion of code associated with the instruction as being a hot spot if the count of the events associated with the execution of the instruction in the hardware counter exceeds the threshold (See column 5, lines 29-30: The best_hint field indicates the current hot spot).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to show further art related to method and apparatus for counting instruction execution and data accesses to identify hot spots:

U.S. Patent # 5,394,529 to Brown, III et al shows a branch prediction unit for high-performance processor.

U.S. Patent # 6,233,679 B1 to Holmberg shows a method and system for branch prediction.

U.S. Patent # 6,662,295 B2 to Yamaura shows a method and system dynamically presenting the branch target address in conditional branch instruction.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
April 6, 2006

Supervisory FRITZ FLEMING PRIMARY EXAMINER GROUP 2100 AU 2181 4/14/2006